AMENDMENTS TO THE CLAIMS:

Please cancel claims 1 – 8 and 17 – 20, without prejudice or disclaimer of their subject matter, and amend claims 9 and 13 – 16 as indicated below. This listing of claims will replace all prior versions and listings of claims in the application:

1. – 8. (Canceled)

9. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a first region and a second region;

a buried insulating film formed in the first region of the semiconductor substrate;

at least one first single crystalline semiconductor layer having a semiconductor element formed therein and formed [[in]] on the buried insulating film [[and]];

at least one second single crystalline semiconductor layer formed in the second region and in contact with the semiconductor substrate; and

an element isolation region for isolating the single crystalline semiconductor layers from each other,

wherein all the element isolation insulating films in the element isolation region have the same height from the semiconductor substrate.

10. (Original) The semiconductor device according to claim 9, wherein the first single crystalline semiconductor layer formed in the first region consists of a plurality of semiconductor layers having a plurality of film thicknesses.

11. (Original) The semiconductor device according to claim 9, wherein a CMOS element is formed in the first region and a bipolar element is formed in the second region.

12. (Original) The semiconductor device according to claim 10, wherein a CMOS element is formed in the first region and a bipolar element is formed in the second region.

13. (Currently Amended) The semiconductor device according to claim 9, wherein a MOS transistor is formed in a predetermined first single crystalline semiconductor layer of the first region; a bipolar transistor is formed in a predetermined second single crystalline semiconductor layer of the second region; the first and second single crystalline semiconductor layers have substantially the same height from the surface of the semiconductor substrate; and the thickness of the semiconductor layer lower than [[the]] a gate electrode of the MOS transistor is substantially the same as the thickness of [[a]] the predetermined second single crystalline semiconductor layer.

14. (Currently Amended) The semiconductor device according to claim 10, wherein a MOS transistor is formed in a predetermined first single crystalline semiconductor layer of the

first region; a bipolar transistor is formed in a predetermined second single crystalline semiconductor layer of the second region; the first and second single crystalline semiconductor layers have substantially the same height from the surface of the semiconductor substrate; and the thickness of the semiconductor layer lower than [[the]] a gate electrode of the MOS transistor is substantially the same as the thickness of [[a]] the predetermined second single crystalline semiconductor layer.

15. (Currently Amended) The semiconductor device according to claim 11, wherein a MOS transistor is formed in a predetermined first single crystalline semiconductor layer of the first region; a bipolar transistor is formed in a predetermined second single crystalline semiconductor layer of the second region; the first and second single crystalline semiconductor layers have substantially the same height from the surface of the semiconductor substrate; and the thickness of the semiconductor layer lower than [[the]] a gate electrode of the MOS transistor is substantially the same as the thickness of [[a]] the predetermined second single crystalline semiconductor layer.

16. (Currently Amended) The semiconductor device according to claim 12, wherein a MOS transistor is formed in a predetermined first single crystalline semiconductor layer of the first region; a bipolar transistor is formed in a predetermined second single crystalline semiconductor layer of the second region; the first and second single crystalline semiconductor layers have substantially the same height from the surface of the semiconductor substrate; and

the thickness of the semiconductor layer lower than [[the]] a gate electrode of the MOS transistor is substantially the same as the thickness of [[a]] the predetermined second single crystalline semiconductor layer.

17. – 20. (Canceled)